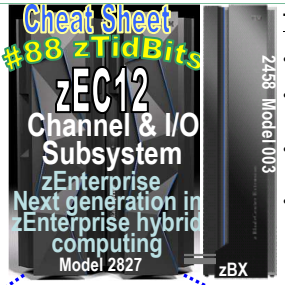


• The **zEC12 I/O subsystem design** provides great flexibility, high availability, and excellent performance characteristics, as follows:
- High bandwidth:
  o The zEC12 uses PCIe as an internal interconnect protocol to drive PCIe I/O drawers. NOTE: The **I/O bus infrastructure** data rate increases **up to 8 GBps**.
  o The zEC12 uses InfiniBand as the internal interconnect protocol to drive I/O cages and I/O drawers and CPC to CPC connection. InfiniBand supports I/O bus infrastructure data rate up to 6 GBps.
- Connectivity options:
  o The zEC12 can be connected to a range of interfaces such as FICON/Fibre Channel Protocol for storage area network connectivity, and for CPC to CPC connectivity by FICON CTCs (FCTC), 10 Gigabit Ethernet, Gigabit Ethernet, and 1000BASE-T Ethernet for local area network connectivity.
- For CPC to CPC connection, zEC12 uses Parallel Sysplex InfiniBand (PSIFB), ISC-3 coupling links.
- Concurrent I/O upgrade:
  o You can concurrently add I/O cards to the server if an unused I/O slot position is available.
- Concurrent PCIe I/O drawer upgrade
- Additional PCIe I/O drawers can be installed concurrently without preplanning if there is free space in one of the frames.
- Dynamic I/O configuration:
  o Dynamic I/O configuration supports the dynamic addition, removal, or modification of channel path, control units, and I/O devices without a planned outage.
- Pluggable optics:
  o The FICON Express8S, FICON Express8, and FICON Express4 features have Small Form Factor Pluggable (SFP) optics to permit each channel to be individually serviced in the event of a fiber optic module failure. The traffic on the other channels on the same feature can continue to flow if a channel requires servicing.
- Concurrent I/O card maintenance:
  o Every I/O card plugged in an I/O cage, I/O drawer, or PCIe I/O drawer supports concurrent card replacement in case of a repair action.

The zEC12 server uses fanout cards to connect the I/O hardware Subsystem to the processor.

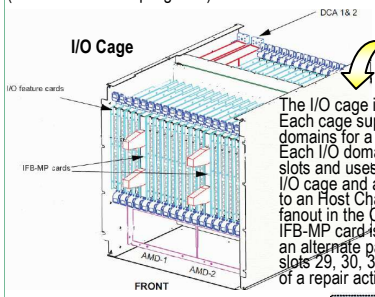
Summary of supported I/O features

- Up to 176 FICON Express4 channels
- Up to 176 FICON Express8 channels
- Up to 320 FICON Express8S channels
- Up to 96 OSA-Express3 ports
- Up to 96 OSA-Express4S ports
- Up to 48 ISC-3 coupling links
- Up to 16 InfiniBand fanouts:
  – Up to 32 12x InfiniBand coupling links with HCA2-O fanout, or
  – Up to 32 1x InfiniBand coupling links with HCA2-O LR (1xIFB) fanout, or
  – Up to 32 12x InfiniBand coupling links with HCA3-O fanout, or
  – Up to 64 1x InfiniBand coupling links with HCA3-O LR (1xIFB) fanout

Enhancements include removing pre-planning requirements with the fixed 32 GB HSA.Customers will no longer need to worry about using their purchased memory when defining their I/O configurations with reserved capacity or new I/O features. Maximums can be configured and IPLed so that insertion at a later time can be dynamic and not require a power on reset of the server.

Coupling links: The maximum number of external coupling links combined (ISC-3 and IFB coupling links) cannot exceed 112 for each zEC12.

InfiniBand (IFB) is a switched fabric communications link used in high-performance computing and enterprise data centers.

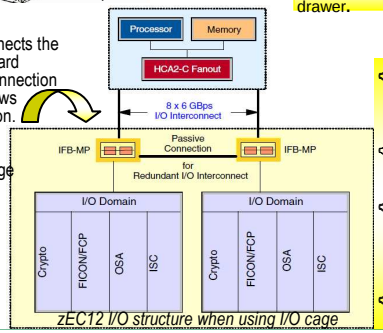


The I/O cage is fourteen EIA units high. Each cage supports up to seven I/O domains for a total of 28 I/O card slots. Each I/O domain supports four I/O card slots and uses an IFB-MP card in the I/O cage and a copper cable connected to an Host Channel Adapter (HCA-C) fanout in the CPC cage. An eight IFB-MP card is installed to provide an alternate path to I/O cards in slots 29, 30, 31, and 32 in case of a repair action.

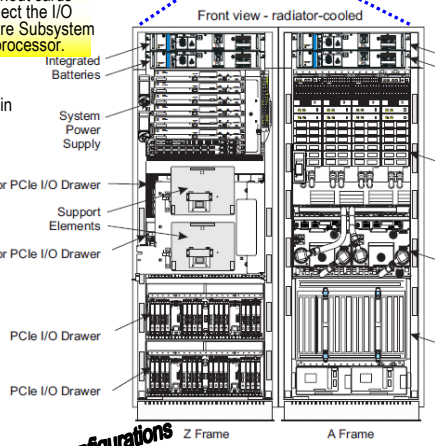
The Flash Express cards are plugged into the PCIe I/O drawer.

• An InfiniBand (IFB) cable connects the HCA2-C fanout to an IFB-MP card in the I/O cage. The passive connection between two IFB-MP cards allows for redundant I/O interconnection.
• The IFB cable between an HCA2-C fanout in a book and each IFB-MP card in the I/O cage supports a 6 GBps bandwidth.

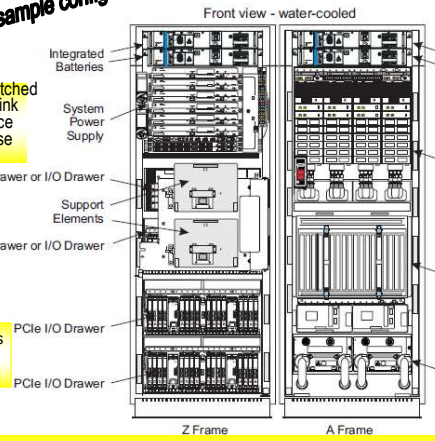
Each I/O domain supports up to four I/O cards (FICON, OSA, Crypto, or ISC). All I/O cards are connected to the IFB-MP cards through the backplane board.



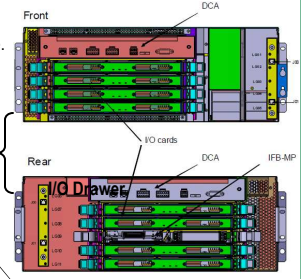
zEC12 I/O structure when using I/O cage



sample configurations

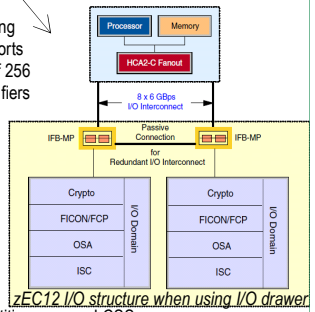


The I/O drawer is five EIA units high and supports up to eight I/O feature cards where each I/O drawer supports two I/O domains (A and B) for a total of eight I/O card slots.
• Each I/O domain uses an IFB-MP card in the I/O drawer and a copper cable to connect to a Host Channel Adapter (HCA) fanout in the CPC cage.
• The link between the HCA in the CPC and the IFB-MP in the I/O drawer supports a link rate of up to 6 GBps.
NOTE: All cards in the I/O drawer are installed horizontally.
• The two distributed converter assemblies (DCAs) distribute power to the I/O drawer. The locations of the DCAs, I/O feature cards, and IFB-MP cards in the I/O drawer are shown on right.
• An IFB cable connects the HCA fanout card to an IFB-MP card in the I/O drawer.
- The passive connection between two IFB-MP cards allows redundant I/O interconnection (RII).
- This provides connectivity between an HCA fanout card, and I/O cards in case of concurrent fanout card or IFB cable replacement.
- The IFB cable between an HCA fanout card and each IFB-MP card supports a 6 GBps link rate.



A **channel subsystem (CSS)** structure for zEC12 is designed for 256 channels. With the scalability benefits provided by zEC12, it is essential that the channel subsystem (CSS) structure is also scalable and permits "horizontal" growth. This is facilitated by allowing more than one logical channel subsystem (LCSS) on a single zEC12.

NOTE: One operating system image supports up to a maximum of 256 Channel Path Identifiers (CHPIDs).



zEC12 I/O structure when using I/O drawer

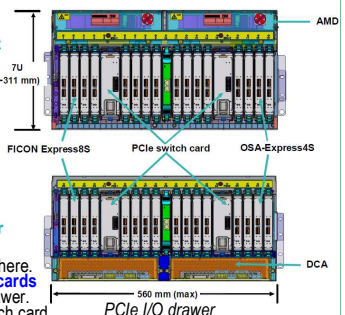
The CSS structure offers the following:
• Four logical channel subsystems (LCSSs)
  – Each LCSS can have up to 256 channels
  – Each LCSS can be configured with one to 15 logical partitions (cannot exceed 60 LPARs per system).
• Spanned channels are shared among logical partitions across LCSSs.
• Channel paths, control units, and devices that can be dynamically added, changed, and deleted in multiple LCSSs.

The **I/O Subsystem (IOSS)** continues to be viewed as a single Input/Output Configuration Data Set (IOCDS) across the entire system with up to four LCSSs.
- Only one Hardware System Area (HSA) is used for the multiple LCSSs.
• A CHPID is a two-digit hexadecimal number that identifies a channel path in the CPC.
- A Physical Channel Identifier (PCHID) is a three-digit number that identifies the physical location (cage, slot, card port) for a channel path in the CPC.
- An adapter ID (AID) is a two-digit hexadecimal number that identifies fanout cards.
  o CHPIDs are associated with ports on an adapter and the AID is used in that definition.
• The CHPID Mapping Tool can help you map your PCHIDs to the CHPID definitions in your IOCP source statements. The tool will provide you with a report with your CHPID assignment in addition to the PCHID value
-The CHPID Mapping Tool is available from Resource Link, *http://www.ibm.com/servers/resourcelink*

The **Multiple Image Facility (MIF)** allows channel sharing among multiple LPARs and optionally shares any associated I/O devices configured to these shared channels. MIF also provides a way to limit the logical partitions that can access a reconfigurable channel, spanned channel, or a shared channel to enhance security.
• With multiple LCSSs, the CSS provides an independent set of I/O controls for each logical channel subsystem called a CSS image. Each logical partition is configured to a separate CSS image in order to allow the I/O activity associated with each logical partition to be processed independently as if each logical partition had a separate CSS. For example, each CSS image provides a separate channel image and associated channel path controls for each shared channel and separate subchannel images for each shared device that is configured to a shared channel.

The **PCIe I/O drawer** attaches to the processor node through a PCIe bus and uses PCIe as the infrastructure bus within the drawer.
• The PCIe I/O bus infrastructure data rate is up to 8 GBps. PCIe switch ASICs Application-Specific Integrated Circuit) are used to fanout the host bus from the processor node to the individual I/O cards. Up to 128 channels (64PCIe I/O features) are supported versus the 112 channels (28 I/O features) offered with the I/O cage.
• The PCIe drawer is **a two sided drawer** (I/O cards on both sides) that is 7U high (one half of I/O cage).
- The drawer contains 32 I/O card slots, four switch cards (two in front, two in rear), two DCAs to provide the redundant power and two air moving device (AMDs) for redundant cooling.
- The locations of the DCAs, AMDs, PCIe switch cards, and I/O feature cards in the PCIe I/O drawer are shown here.
• The PCIe I/O Drawer supports up to **32 I/O cards** organized in four hardware domains per drawer.
- Each domain is driven through a PCIe switch card.
- Always two PCIe switch cards provide a backup path for each other through the passive connection in the PCIe I/O Drawer backplane, so that in case of a PCIe fanout card or cable failure, all 16 I/O cards in the two domains can be driven through a single PCIe switch card.

All I/O cards are connected to the PCIe switch card through the backplane board.



PCIe I/O drawer

☛ The zEC12 supports a PCIe I/O and InfiniBand infrastructure. PCIe features are installed in PCIe I/O drawers. In addition, when carried forward on an upgrade from a z196 or z10™ EC, up to two I/O drawers, which were introduced with the IBM z10 BC, and one traditional I/O cage are also supported.
☛ There are up to 48 high-performance fanouts for data communications between the server and the peripheral environment. The multiple channel subsystems (CSS) architecture allows up to four CSSs, each with 256 channels.
☛ For I/O constraint relief, three subchannel sets, are available per CSS, allowing access to a greater number of logical volumes. for improved device connectivity for Parallel Access Volumes (PAVs), PPRC secondaries, and FlashCopy® devices; this third subchannel set allows the user to extend the amount of addressable external storage. The zEC12 allows to IPL from subchannel set 1 (SS1) or subchannel set 2 (SS2), in addition to subchannel set 0.
☛ In addition, the system I/O buses take advantage of the PCIe technology and of InfiniBand technology, which is also exploited in coupling links.